REMARKS

With the foregoing amendment, Claims 1-17 remain pending in the application. Claims 1, 6, 8, 12, and 13 have been amended. The Applicants respectfully traverse the Examiner's rejection under 35 U.S.C. § 103.

In the non-final Office Action, Claims 6 and 12 were objected to because of typographical errors with respect to the term "milli." The Applicants appreciate the Examiner's observations and have amended Claims 6 and 12 accordingly to address the Examiner's objections.

The Examiner rejected Claims 1-17 under 35 U.S.C. § 103(a) as being unpatentable over Duggan et al. (U.S. Patent No. 6,359,942) in view of Lee et al. (U.S. Patent No. 6,014,768). The Applicants respectfully disagree.

The Applicants have amended base Claims 1, 8, and 13 to more clearly state that the plurality of differential threshold signals are "dependent on a substantially constant reference signal" (See Claims 1, 8, and 13) which is supported in the Application, as originally filed, on page 9, lines 4-14 and Fig. 4B, among other locations. At the time the Application was filed, it was known in the art that a bandgap reference generator, e.g., bandgap reference 512 (See Application, Fig. 4B), provides a substantially constant reference signal, e.g., a constant direct current voltage, regardless of variations in circuit temperature among other factors.

The present invention includes a method for recovering data encoded in a received signal using a slicer circuit by generating a plurality of differential threshold signals dependent on a substantially constant signal reference. The slicer circuit couples one of the differential threshold signals to the inputs of a first differential amplifier. The slicer circuit also couples a differential input signal to the inputs of a second differential amplifier where the second differential amplifier is cross-coupled to the first differential amplifier. The slicer circuit then

outputs a differential output signal that is dependent on the difference between the differential threshold signal and the differential input signal.

Duggan et al. describe a frequency shift key (FSK) demodulator for demodulating the I and Q output signals provided by a direct conversion receiver arrangement. Duggan et al. further describe a data slicer 5 (See Fig. 5) that includes three "digital comparators" (col. 3, lines 20-41). The digital comparators compare "digital values from respective threshold registers N1, N2, and N3 with the value present on an "N-bit path 4" (See col. 2, line 54). Unlike analog comparators, the digital comparators compare the N-bit digital data on path 4 with the N-bit digital data in the registers N1-N3. The digital data settings for N1-N3 are derived from the MAX register 30 (See col. 2, lines 49-67) and MIN register 34 (See col. 3, lines 1-4) settings (See col. 3, lines 25-32). Because the MAX and MIN register values are dependent on the "incoming signals from the FIR filter 3" (See col. 2, lines 53-55) and can vary with respect to time, the values in registers N1-N3 can vary with depending on value of the incoming signal from the FIR filter 3.

Lee et al. describe a method and apparatus for monitoring a read channel in a disk drive system and calibrating the disk drive system. The monitoring apparatus includes a slicer circuit that generates an ideal signal based on the signal 300 (See Fig. 3) detected from the read channel. Then a window generator uses the idea signal to generate a moving signal envelope (or window) including an upper limit 400 and lower limit 401 (See Fig. 4). Then, comparators 112 and 113 (See Fig. 1) compare the received signal 300 with the upper and lower limits 400 and 401 to determine whether the read channel quality is within the acceptable envelope. A counter is used to track the number of times the signal 300 falls outside the envelope. The comparators 112 and 113 compare the sampled data 100 with top and bottom reference voltages via lines 107 and 108 respectively. The voltage Vref is derived from the varying ideal sample reference signal

(col. 7, lines 35-38). Because the reference voltages on lines 107 and 108 are dependent on the varying Vref (See Figs. 5a and 5b), the reference (threshold) voltages do not remain constant and vary according to the detected idealized sample reference.

The Examiner admits that Duggan et al. "failed to teach a differential comparator" including differential amplifiers (See Office Action, Page 2). While Duggan et al. describe digital threshold registers N1, N2, and N3 which are dependent on a varying signal from the FIR filter, Duggan et al. neither teach nor suggest using differential threshold signals that are "dependent on a substantially constant reference signal" as claimed in amended base Claims 1, 8, and 13. While Lee et al. describe a differential comparator using threshold voltages derived from a varying Vref signal, Lee et al. neither teach nor suggest using differential threshold signals that are "dependent on a substantially constant reference signal" as claimed in base Claims 1, 8, and 13.

Because Duggan et al., Lee et al., or their combination do not add the use of differential threshold signals that are dependent on a substantially constant reference signal, the combination of Duggan et al. and Lee et al. does not make a case of prima facie obviousness regarding the invention as claimed in base Claims 1, 8, and 13.

According to the Examiner, "it would be obvious to an ordinary skilled in the art at the time the invention was made to use Lee et al.'s differential comparator in Duggan et al.'s slicer to generate an ideal waveform that tracks the input" (See Office Action, Page 3). The Applicants respectfully disagree. The present invention is concerned, at least in one embodiment, with reducing the effects of common mode voltages on a slicer circuit (See Application page 2, lines 7-14) by using, along with other features, threshold voltages that are dependent on a substantially constant reference signal. There is no suggestion or motivation in

Duggan et al. and Wong et al. to utilize threshold voltages dependent on a substantially constant reference signal.

Because there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill on the art, to modify and/or combine Duggan et al. with Lee et al. to realize the invention as claimed in amended base Claims 1, 8, and 13, the combination of Duggan et al. and Lee et al. does not make a case of prima facie obviousness regarding the invention as claimed in Claims 1, 8, and 13.

Therefore, the rejection of base Claims 1, 8, and 13 under 35 U.S.C. § 103 should be withdrawn.

Because Claims 2-7, 9-12, and 14-17 are dependent on and limited by now allowable base Claims 1, 8, and 13, the rejection of these dependent Claims should be withdrawn.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Applicants believe that the appropriate fees are provided due in connection with this submission. However, if an additional fee is due, please charge our Deposit Account No. 18-1945, under Order No. NNET-P01-022 from which the undersigned is authorized to draw.

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Respectfully submitted,

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